# Design of an On-Chip SIDO Step-Down Converter with Independent Outputs

Herminio Martínez-Garcia[(1)], Jose Silva-Martinez[(2)]

[(1)] Barcelona College of Industrial Engineering (EUETIB)
Department of Electronics Engineering
Technical University of Catalonia (UPC). BarcelonaTech
C/ Comte d'Urgell, nº 187. E-08036 - Barcelona. SPAIN
herminio.martinez@upc.edu

[(2)] Analog and Mixed Signal Center
Electrical and Computer Engineering Department (ECE)
Texas A&M University
College Station, TX, 77843-3128, USA
jsilva@ece.tamu.edu

***Abstract*— The portable electronics market is rapidly migrating towards more compact devices requiring multiple high-integrity high-efficiency voltage supplies for empowering the systems. This paper demonstrates a single inductor used in a buck converter with two output voltages from an input battery with voltage of value 3 *V*. The main targets are low cross regulation between the two outputs to supply independent load current levels while maintaining desired output voltage values well within the acceptable ripple levels. The proposed controller provides adaptive levels in order to limit the output ripple, achieving a high output voltage accuracy. A reverse current detector to avoid negative current flowing through the inductor, prevents possible efficiency degradation.**

***Keywords—CMOS Technology; DC-DC Converters; Single Inductor Dual Output (SIDO) DC-DC Converters; Cross-regulation.***

## I. INTRODUCTION

Switched mode power supplies (SMPSs) are required in electronic devices such as cellular phones, laptops, etc. SMPS's are preferred to linear regulators due to higher efficiencies attained. The SMPS consists of switches, inductors and capacitors that serve the purpose of filtering high frequency switching currents. However, a major disadvantage of using SMPS for multiple outputs are high area and cost associated with the passive filter components. The typical buck converter (shown in Fig.1) is the most frequently used switching converter in portable applications. For the buck converter shown in Fig. 1, the inductance required for the design parameters current ripple, input battery voltage, switching frequency and desired output voltage can be approximated as [1]:

$$L = \frac{V_1(1-\frac{V_1}{V_{bat}})}{\Delta i_L f_s}, \qquad (1)$$

where $f_s$ is the switching frequency of synchronous switches *Sp* and *Sn* and $\Delta i_L$ is the desired inductor ripple current. Although it depends on the particular application, usually the current ripple $\Delta i_L$ is chosen to be around 5-10% of the DC load current $I_o$. According to (1), the lower the inductor's ripple current, the higher the value of the inductance required. Since multiple voltage rails are required on a Power Management IC (PMIC), several such converters are normally used in a device for obtaining different voltage levels. If a PMIC supplies $N$ independent voltage rails, $N$ such converters might be required. The costliest and most area consuming component on the board of a SMPS design is the inductor. A solution for this issue is to use a single-inductor serving to multiple outputs [2-8]. Since the inductor is shared, the minimization of cross-regulation is highly desirable to maintain the regulator's outputs independent of each other. Although the focus of this paper is to demonstrate that a single inductor can also be used for two independent (low cross regulation) outputs in a buck SMPS, the concept can be easily extended for higher number of independent outputs.

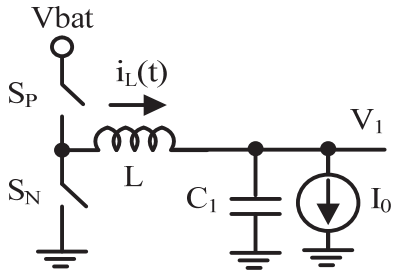


Figure 1. Topology of the basic buck converter.

## II. SIDO BUCK CONVERTER CONTROL

The topology of the single-inductor dual output (SIDO) buck converter is shown in Fig. 2 where two independent outputs $V_1$ and $V_2$ are obtained from a single inductor $L$. $C_1$ and $C_2$ are output capacitors that maintain average load voltages $V_1$ and $V_2$ respectively, and provide output current when the inductor is serving the other output. The signals $V_{1,2upDC}$, $V_{1,2lowDC}$, $V_{1,2up}(t)$ and $V_{1,2low}(t)$ are described in the following subsections. In order to design the inductor for the minimum possible ripple current (1) can be extended to the SIMO buck converter with $N$ outputs and the value of the inductance is chosen to limit the ripple current within the specifications as follows:

$$L = \max\left(\frac{V_1 T_1(1-\frac{V_1}{V_{bat}})}{\Delta i_L}, \ldots, \frac{V_N T_N(1-\frac{V_N}{V_{bat}})}{\Delta i_L}\right), \qquad (2)$$

where $\Delta i_L$ is the minimum current ripple and $T_1$, $T_2$, … and $T_N$ are the time windows for which $L$ is connected to the outputs $V_1$, $V_2$, … $V_N$, respectively. Instead of using $N$ inductors of different values, a single inductor selected to satisfy the maximum allowable value ensures minimum ripple current excursion.

The timing diagram in Fig. 2 shows the different phases of operation of the SIDO buck converter. The slopes of inductor charge and discharge depend on the output that $L$ is connected to for regulation. The time frames $T_1$ and $T_2$ depend on the load demanded at each output and are adjusted interactively by the feedback dynamic level comparator. The time periods $T_1$ and $T_2$ are adjusted by the controller such that the average loads at both outputs are delivered over one time period when the converter is in steady state; i.e.:

$$\frac{\int_0^{T_1} i_l(t)dt}{T_1+T_2} = i_{1average} \qquad \frac{\int_{T_1}^{T_2} i_l(t)dt}{T_1+T_2} = i_{2average} \tag{3}$$

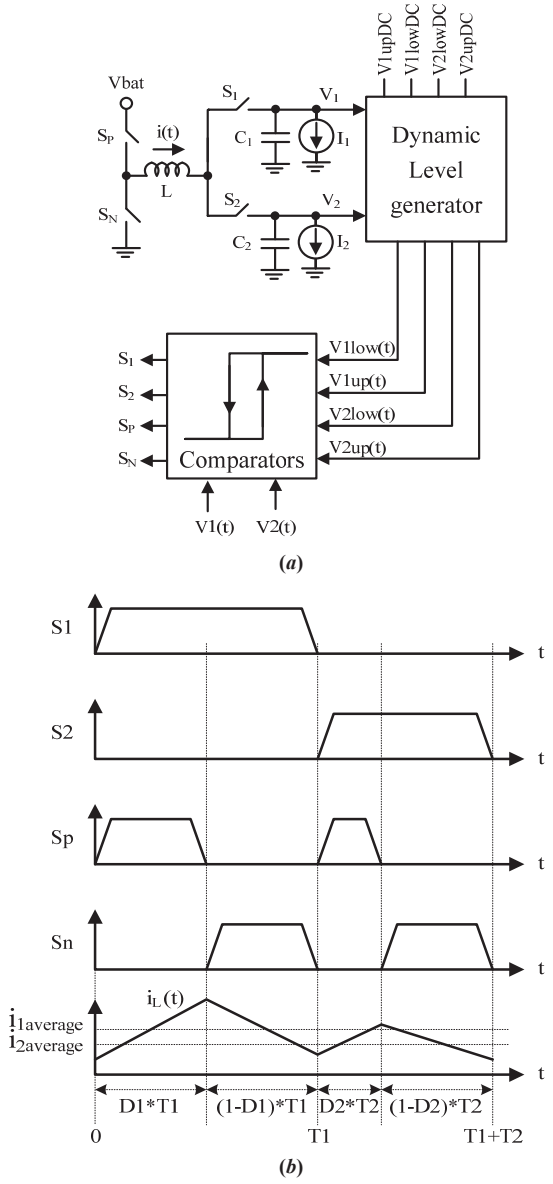


Figure 2. (*a*) SIDO Buck Converter SMPS. (*b*) Timing Diagram.

The issue of cross-regulation arises from the sharing of boundary conditions of inductor current between the output branches. This causes coupling between the sub converters. If the inductor were to discharge to a state of zero current at the end of every time window, then independent load supply can be achieved at each output without undesirable rise or fall in voltage [2-5]. However, the disadvantage of operating the SIDO buck converter in this mode of discontinuous conduction for all load conditions is the rise in peak currents flowing through the inductor, increasing current stress of the switches and conduction losses [1] as well as loss in system efficiency due to the full charge and discharge of additional parasitic capacitors. To decrease the peak inductor currents the inductor might be reset to a constant value $I_{dc}$ instead of zero [6-7]. A variation of this technique is to reset the inductor to different current values that are dependent on the individual loads. This technique requires an additional low-resistance switch across the inductor. Further, current sensing circuits that are sensitive to high frequency noise are required. Control methodologies like Adaptive Delta Modulation [8] and Ordered Power Distributive Control [9] use digital algorithms and analog signal processing circuits to control the voltages. These solutions have a fixed frequency of operation. This leads to the inability of the SIMO SMPS to regulate with wide load ranges at both outputs.

### *A. Proposed Hysteresis Control*

In this work, the problem of cross-regulation is overcome by having variable frequency of operation. The conditions stated in (3) can be met irrespective of the boundary condition of inductor current i.e. irrespective of load level at the outputs. The proposed controller for the SIDO buck converter is able to supply the output at full load as well as the output at stand-by simultaneously without the undesirable drop or rise respectively in voltage levels at either output. Dynamic (time varying) levels that contain information about the slopes of the output voltages are used for providing an indication of the voltages and load currents at the outputs. The first derivative of the voltage indicates the amount of load present at the outputs. For each output, two dynamic levels $V_{1,2up}(t)$ and $V_{1,2low}(t)$ are properly defined and serve as thresholds against which the SIDO buck outputs are compared so that the voltage ripples are limited to within 10% of the reference voltages under all loading conditions. Let us define $V_{1,2upDC}$ and $V_{1,2lowDC}$ as the bounds for the SIDO buck's outputs $V_{1,2}$. The dynamic threshold voltage levels are defined as follows:

$$V_{1,2up}(t) = V_{1,2upDC} - K_z \cdot \frac{dV_{1,2}(t)}{dt} \tag{4}$$

$$V_{1,2low}(t) = V_{1,2lowDC} - K_z \cdot \frac{dV_{1,2}(t)}{dt} \tag{5}$$

The derivative of the output voltages is a measure of inductor current; hence the threshold levels are dynamically adjusted according to $I_L$. The value of coefficient $K_Z$ determines the sensitivity of the dynamic levels. A very large $K_Z$ causes high swing in the upper and lower dynamic levels and possibly their overlap whereas a small value desensitizes the threshold levels to load current variations increasing the output voltage ripple.

The output voltages $V_{1,2}$ are limited to the hysteresis bands by comparing them with the dynamic levels to control the switches $S_P$ and $S_N$. As shown in Fig. 3, by monitoring the output voltage and its first derivative, the transient response is improved the ripple is limited around the desired DC value. While serving one of the outputs, $S_P$ is activated and the voltage variation is positive due to the current injected by the inductor. Based on the speed of the variation of the output voltage, the dynamic level is adjusted;

large load current leads to large steps in the dynamic levels. Since $I_L$ is positive, the threshold voltage $V_{1,2up}$ decreases thus preventing significant overshoot at the end of the $S_P$ phase even in the presence of control circuit delays. In the following $S_N$ phase one of the inductor terminals is grounded but continues to serve the output. During $T_2$, the output voltage discharge at a rate given by $-I_{1,2}/C_{1,2}$. This causes a step increase in the dynamic levels, making it move closer to the output voltage profile. When switching from one output to the other, switch $S_1$ is closed if the voltage $V_1$ discharges to below $V_{1low}(t)$; i.e. $S_1$ and $S_2$ are controlled by load levels in the outputs. This guarantees that $V_1$ and $V_2$ stays well within the static bounds $V_{1,2upDC}$ and $V_{1,2lowDC}$.

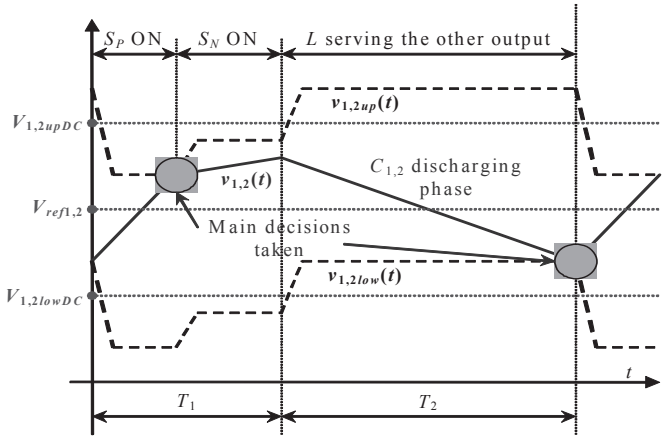


Figure 3. SIDO's steady state output and corresponding dynamic thresholds.

### B. *Control operation flowchart*

The flowchart shown in Fig. 4 summarizes the sequence of operations implemented by the digital controller. The flag 'M' and reverse current flag 'R' are used by the controller to decide the states of $S_1$ and $S_2$. Once the inductor is connected to a particular output, the voltage is compared to corresponding dynamic levels for manipulation of $S_p$ and $S_n$. $S_p$ is switched ON when the voltage goes below the lower dynamic threshold and $S_n$ is turned ON when the voltage overshoots the upper dynamic threshold. Thus asynchronous control of the SIDO buck converter is established through variable frequency control pulses that manipulate the power switches. The comparators and digital logic ensures that the output with higher error and higher load current gets the higher priority.

### C. *Architecture and control system*

Fig. 5 shows the topology and control architecture of the SIDO buck converter. Eqns. (4) and (5) are implemented using analog differentiators with DC offsets. $V_1$ and $V_2$ are compared with the dynamic levels to generate the control signals for switches $S_p$ and $S_n$. $S_1$ and $S_2$ are controlled by the priority comparator's output. The digital control block uses the signal priority flag M and control signal $V_{1,2low}$ to handle $S_{1,2}$ appropriately. Reverse current is detected monitoring $S_1$ and $S_2$ in order to avoid the flow of negative current flowing through the inductor. When the reverse current detector 'R' is high the switches $S_n$ and $S_{aux}$ are closed while all the other switches are immediately turned OFF. This switching action grounds the inductor terminals avoiding negative current flow through it and also prevents efficiency degradation.

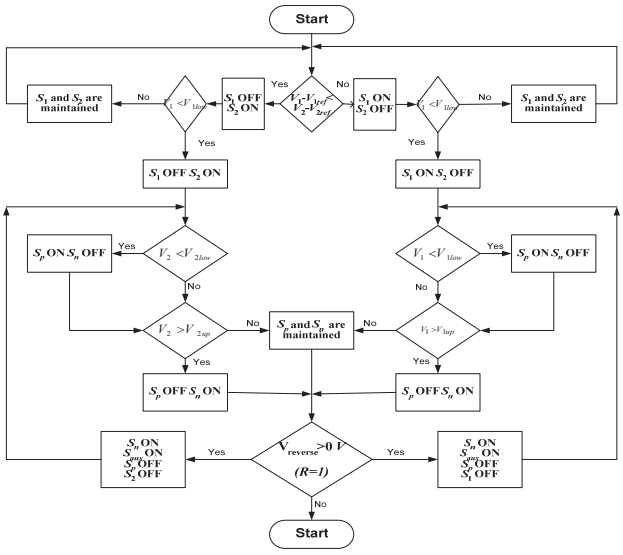


Figure 4. Logical flow of operations in the SIDO Buck Converter.

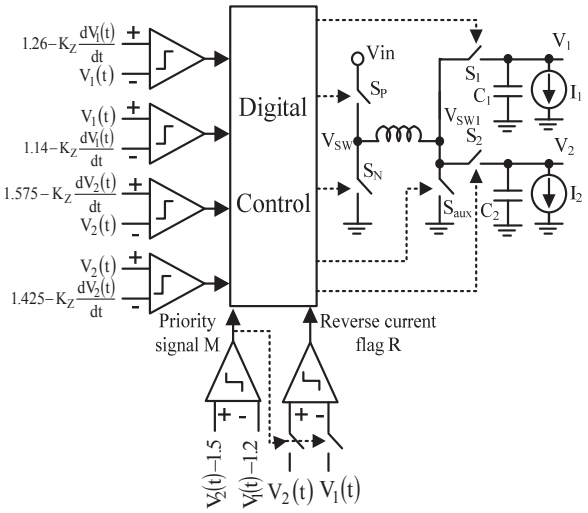


Figure 5. SIDO system Overview.

## III. SCHEMATIC SIMULATION RESULTS

In this work, the value of $L$ is1 µH and the values of the output capacitors are 4.7 µF each. The controller was designed and simulated at transistor level using a conventional 0.5 µm CMOS technology. When maximum load i.e. 300 mA is present at each output, the transient response of $V_1(t)$ and $V_2(t)$ with corresponding dynamic levels are shown in Fig. 6. Overshoots or undershoots about their designated static bounds are due to the response time of the loop control. In Fig. 7, the load at $V_1(t)$ is 10 mA and at $V_2(t)$ is 300 mA. In the circled area in Fig. 7, $S_1$ stays ON for just as long as the capacitor $C_1$ gets charged to over $V_{1low}$. Once the light load output $V_1$ is charged over its acceptable lower limit, the inductor is immediately connected to the output $V_2$ with the heavier load, and the switches $S_p$ and $S_n$ continue to get manipulated according to the dynamic thresholds. Hence both

outputs with widely varied load values are served by the inductor thus minimizing the cross regulation.

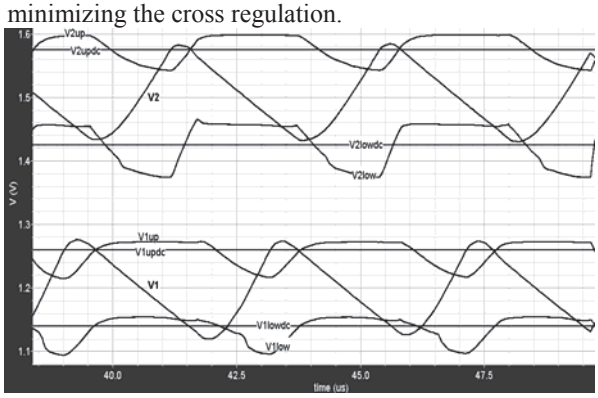


Figure 6. Steady state $V_1$ and $V_2$ when load currents $I_1$=$I_2$=300 *mA*.

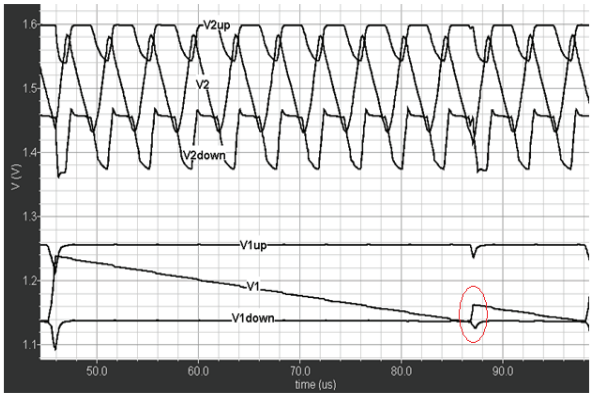


Figure 7. Steady state $V_1$ and $V_2$ when load currents $I_1$=10 *mA* and $I_2$=300 *mA*.

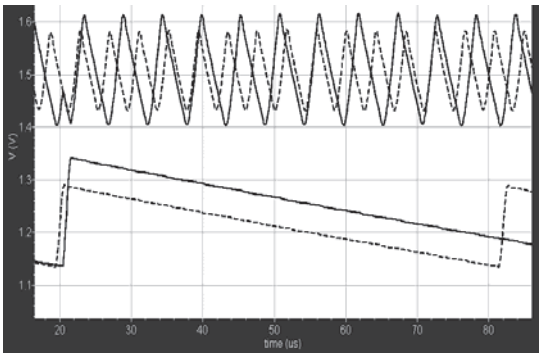


Figure 8. Comparison of static and dynamic hysteresis.

Fig. 8 shows two families of curves; the dotted traces correspond to the output voltages with dynamic hysteresis, while the solid lines indicate the outputs with static hysteresis. When dynamic levels are used the voltage ripple is better controlled within the permissible bounds. In the case of static hysteresis, a large output capacitor would be required to effectively control this ripple value. Fig. 9 shows the load regulation of $V_1(t)$ and cross regulation of $V_2(t)$. There is a step increase in the load current $I_1$ from 10mA to 300mA leading to an increase in the ripple frequency of $V_1(t)$ at the instant of the load step. This increase in the switching frequency ensures that the sudden load step is handled by the inductor energy, thus helps the loop recover without any undesirable dips in the output voltages.

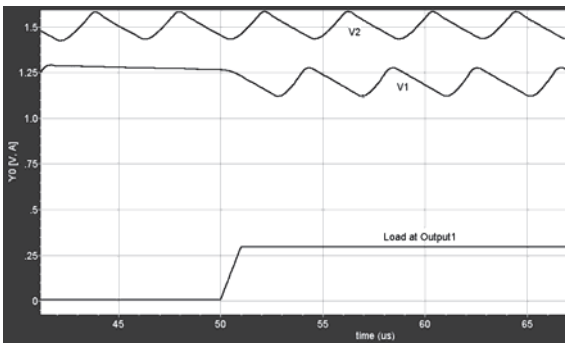


Figure 9. Time response of $V_1$ and $V_2$ to load step from 10 *mA* to 300 *mA*.

## IV. CONCLUSION

A single-inductor two-output switching regulator with low cross regulation, high accuracy and 10% ripple limits has been described. These achievements are a result of the proposed non linear hysteresis control applied to the SIDO buck converter leading to superior transient performance and disturbance rejection. Using the proposed dynamic hysteresis control methodology, constant efficiency values at different load combinations that is essential for optimum performance is achieved. The downside of the proposed method is the variation of the operating frequency with load. Nevertheless, the switching frequency can be controlled to stay within a band of acceptable frequencies by tuning the width of the hysteresis loop using an auxiliary feedback loop.

## ACKNOWLEDGMENT

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